REMARKS

This case has been carefully reviewed and analyzed in view of the Office Action dated 2 September 2004. Responsive to the Office Action, Claims 1 – 8 are now amended for further prosecution. It is believed that with such amendment of claims, there is a further clarification of their recitations.

In the Office Action, the Examiner rejected Claims 1 – 8 under 35 U.S.C. § 101 stating that the claimed invention is directed to non-statutory subject matter. More specifically, the Examiner stated that the claimed method simply implements a mathematical algorithm for computing a square root of long-bit numbers. The Examiner dismissed the recitation of "a short-bit processor" in the preamble, concluding such to be a mere recitation of intended field of use and not sufficiently tied to a certain computer.

Claims 1 – 8 have now been amended to more clearly recite Applicant's inventive method which, among other things, enables a short-bit processor to quickly and conveniently process a long-bit number – a processing task that would otherwise require (in the absence of a long-bit processor) extensive memory to store data for look-up tables, or else necessitate burdensome processing delays to accommodate an excessive number of computations. As each of the newly-amended independent Claims 1 and 5 now more clearly recites, Applicant's method avoids these drawbacks and enables the use of a short-bit processor in this

regard, "with minimal processing and memory load." Each newly-amended independent claim accordingly recites among its combination of steps such features as "representing" both "the long-bit number ... and a square root solution thereof" as "parametric combination[s] of short-bit data components defined" as respectively specified. The method further recites such other features as "executing in the short-bit processor a digital computation in accordance with" an accordingly defined "successive substitution condition," as well as "recursively executing to convergence ... [this] successive substitution computation," in generating a solution with minimal consumption of processing and data memory resources.

Applicant's claimed method is hardly a pure mathematical algorithm. Hence, the alphanumeric characters used in expressing the mathematical relationships between certain parametric elements are more than mere algebraic variables. They actually represent certain types of data components - namely, "short-bit data components" of certain "parametric combination[s]," as the claims recite – which are to be stored and manipulated by the short-bit processor. They are used by the claimed method to carry out practical applications like a "real-time CD/DVD tracking process," as clarified in each of the Claims 1 and 5 and illustratively described at page 6, line 9 – page 7, line 1 of the Specification, amply meeting the statutory requirement of 35 U.S.C. § 101. The newly-amended Claims clearly set forth, at the very least, statutory subject matter.

It is respectfully submitted, therefore, that the Examiner's basis for rejection of Claims 1 – 8 is now obviated by the clarifying amendments incorporated hereby. Accordingly, it is believed that the subject Patent Application has now been placed fully in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

For: ROSENBERG, KLEIN & LEE

Jun Y. Lee
Registration #40,262

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Rosenberg, Klein & Lee
Suite 101
3458 Ellicott Center Drive
Ellicott City, MD 21043
(410) 465-6678

Customer No.
04586